UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,974	11/08/2001	Ivo Wilhelmus Johannes Marie Rutten	US 018179	2642

7590 09/30/2003

Corporate Patent Counsel
U.S. Philips Corporation
580 White Plains Road
Tarrytown, NY 10591

EXAMINER
PERT, EVAN T

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,974	RUTTEN, IVO WILHELMUS JOHANNES MARIE	
	Examiner	Art Unit	
	Evan Pert	2829	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The specification is objected to for the informality at p. 1, line 23 reading "One of the particularly problems..."

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the reference signs "206", "290", "351", "470a", "470d" and "470e", not mentioned in the description.

Claim Objections

3. Claim 2 is objected to because "configure to" in line 4 should read --configured to--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

"Integrated Circuit"

Applicant uses "integrated circuit" in the claims to describe the circuitry for "preconditioning" such as the configurable monolithic integrated circuit chip depicted in Fig. 5.

Yet, the Authoritative Dictionary of IEEE Standards Terms defines an "integrated circuit" broadly as "a combination of interconnected circuit elements inseparably associated on a continuous substrate" [p. 570]. Here, the substrate could presumably be a "printed wiring board" with components mounted inseparably on the board.

For purposes of examination, the claimed "preconditioning integrated circuit" could be any circuitry or chip functioning on a board near the DUT that performs some kind of conditioning, such as part of conditioning pin electronics of a probe card.

"Immediate Proximity," "Immediately Proximate," and "proximate connection"

The term "proximate" broadly means "very close" according to Merriam-Webster. Applicant seemingly wants to specifically describe the proximal relationship between the "Pre-conditioning IC" and the "DUT" as depicted in Fig. 5. That is, an IC chip is clearly "immediately proximate" a DUT when a major plane of the IC chip is brought toward a major plane of the DUT wherein contact is established by conductive features sandwiched between the planes of the DUT and chip being brought together.

However, since "proximate" simply means "close" in a broadest reasonable interpretation, the intended scope of configuration of pre-conditioning IC circuitry in relationship to the DUT is not clear. For example, a well-known test head with integrated circuit chips as part of pin electronics can be considered "immediately proximate" a DUT. Does applicant intend to mean that IC circuitry in a test head or as part of a probe card is "proximate" in the scope of the claims?

For purposes of examination, "proximate" is interpreted simply as "near" or "close", rather than being immediately juxtaposed as in the exemplary embodiment depicted in Fig. 5.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 3, 7, 11 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Conner et al. (U.S. 6,486,693), in view of the rejections under 35 USC 112 set forth above.

Regarding claim 1, Conner et al. disclose a test system comprising: automated test equipment that includes: a computer that is configured to execute a sequence of test operations (110) for testing a device-under-test (120), and an interface circuit (112, 116), operably coupled to the computer, that is configured to transmit test signals in dependence upon the sequence of test operations that are executed by the computer (col. 3); and a preconditioning integrated circuit (122), operably coupled to the automated test equipment, that is configured to receive the test signals, and to generate therefrom at least one preconditioned test signal that is communicated to the device-under-test; wherein the preconditioning integrated circuit is located in immediate proximity to the device under-test (conditioned with respect to clock "skew"), and includes at least one contact point that is arranged to provide direct contact to the device-under-test for communicating the at least one preconditioned test signal to the device under-test (wherein "direct contact" is necessarily required for electrical *connection* such as to the pins visible on DUT package 120).

Regarding claim 2, the automated test equipment (110) is also configured to receive at least one test response from the device-under-test col. 3, line 30), and the preconditioning integrated circuit (122) is also configured to receive a response signal from the device-under-test via an other contact point (Fig. 2), and to generate therefrom the at least one test response for communication to the automated test equipment (i.e. "measuring").

Regarding claim 3, a probe card (118), upon which the preconditioning integrated circuit (120) is mounted, that facilitates coupling of the preconditioning integrated circuit to the automated test equipment (Fig. 1).

Regarding claim 7, the integrated circuit 122 includes at least an "amplifier" (e.g. 310A).

Regarding claim 11, Conner et al. discloses a preconditioning integrated circuit comprising: a plurality of conditioning elements (part of 116 and 122), each conditioning element includes circuitry that facilitates a conditioning of a test signal that is communicated from an automated test equipment, to form a conditioned test signal that is communicated to a device-under-test (by way of cable assembly 112), and wherein the preconditioning integrated circuit is configured to be located immediately proximate to the device-under-test when the conditioned test signal is communicated to the device-under-test (i.e. the DUT 120 is very close to the conditioning integrated circuitry 116 as seen in Fig. 1).

Regarding claim 17, Conner et al. discloses a method of testing, comprising: programming an automated test equipment (110) to execute a sequence of test operations for testing a device-under-test (120) via a transmission of test signals to a preconditioning integrated circuit (116), and providing the preconditioning integrated circuit that is configured to receive the test signals, and to generate therefrom at least one preconditioned test signal that is communicated to the device-under-test via a proximate connection to the device-under-test (Fig. 1).

Allowable Subject Matter

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior art fails to disclose a configurable monolithic preconditioning integrated circuit for ATE wherein the configurable monolithic preconditioning integrated circuit is brought into direct electrical contact with the DUT by juxtaposing surface contacts of the preconditioning IC with surface contacts of the DUT, as exemplified by arrow 490 depicted in figure 4.

Applicant's configurable preconditioning IC, exemplified by Figs. 5, 6A and 6B, allows a single type of preconditioning IC to be used in ATE for a variety of devices, simply by appropriately configuring the preconditioning IC as exemplified by Fig. 6B.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:30AM-3:30 PM). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

ETP
September 22, 2003

EVAN PERT
PRIMARY EXAMINER